Gate Dielectric Engineered Nanowire MOSFET for Better Reliability

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Abstract

Nanowire MOSFET has attracted a lot of interest due to its enhanced gate control which helps in reducing short channel effects. Apart from short channel performance assessment, reliability assessment is equally important. Assessment of Reliability is important for miniaturized devices as device degradation can lead to instability in circuit performance of the device. Localised charges present at the interface lead to significant variation in electrical performance parameters such as threshold voltage, off current, on current etc. This paper presents an investigation study of methods to improve reliability of Nanowire MOSFET in presence of localized charges. Impact of localized charges on the subthreshold behavior (threshold voltage variation, degradation in I_{on}/I_{off} ratio) can be subdued using gate dielectric engineering i.e. 8 times less degradation for HfO_2 gate dielectric has been observed as compared to SiO_2 dielectric. Effect of other device parameters such as channel radius and dielectric thickness has also been discussed.

Introduction

Nanoscale Nanowire MOSFET with cylindrical geometry has gained a lot of attention as it exhibit enhanced immunity against short channel effects because of its surrounding gate structure which gives better electrostatic control of the channel. Nanowire MOSFET makes possible extending further device scalability. Because of its surrounding gate structure, it offers excellent subthreshold and analog performance. There are many research papers available which suggest the improved short channel performance of Nanowire MOSFET as compared to conventional MOSFET. This paper presents gate dielectric engineered Nanowire MOSFET with Localised interface charges. Gate Dielectric engineering i.e. high-k dielectric in place of standard SiO_2 is one of the popular technique to further extend the scalability of gate dielectric thickness [21],[22]. High-k dielectric helps in reducing gate dielectric thickness without increase in associated gate leakage currents. This paper illustrates the use of gate dielectric engineering for better immunity against interface Localised charges. High-k dielectric leads to lesser degradation in subthreshold performance of Nanowire MOSFET. Impact of other device parameters such as dielectric thickness and channel radius has also been studied through simulations.

Design/Other information

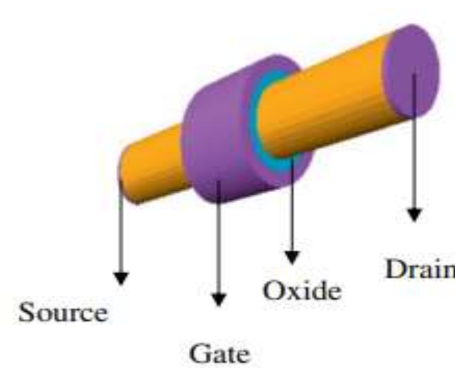

Fig. shows the 3D structure of the simulated device.

- ATLAS-3D device simulator is used to simulate Nanowire MOSFET with interface localised charges.
- Device parameters are: Channel Length (L)=100nm, Channel Radius (R)=20nm, Thickness of Gate Dielectric (t_{ox})=5nm, Substrate Doping (N_a)=$10^{21}m^{-3}$, Source/Drain Doping (N_d)= $10^{26}m^{-3}$.
- INTERFACE statement is used to incorporate the effect of localized charges during the simulation. Density of localized charges is taken to be $\pm 10^{12}$ cm^{-2} .
- For carrier statistics, Boltzmann Model is used. For Carrier Transport, Drift–Diffusion (DD) model is used along with Concentration dependent mobility and Field Dependent Mobility models.
- The standard Shockley–Read–Hall (SRH) recombination model is used to account for Carrier Generation and Recombination processes.
- Quantum models i.e. Quantum effects are not considered as the channel radius is 20nm and quantum effects come into the picture when radius is equal to or less than 5 nm.
- Calibration of simulation results are done with experimental results.

Set up

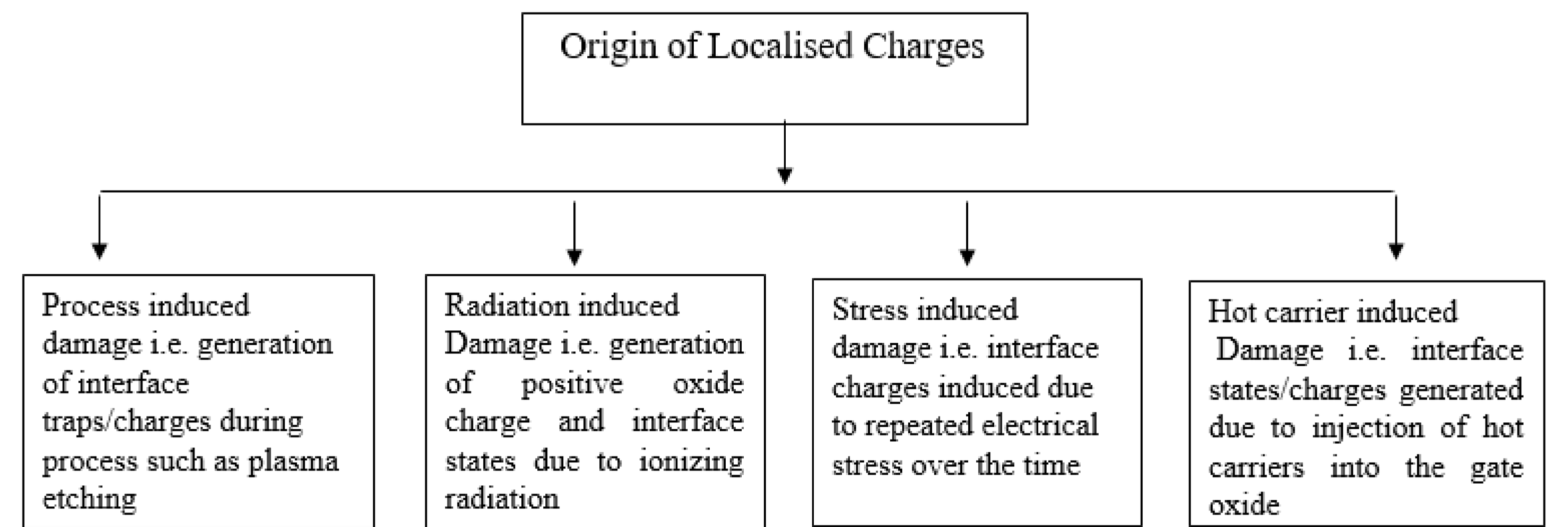

Fig. Different damage mechanisms.

Results

Table.1 Effect of Localised Charges on the Subthteshold behaviour of Nanowire MOSFET. Drain to Source Voltage V_{ds}=0.1V.

Density of Localised Charges (cm^{-2})	Threshold Voltage (V)	I_{on}/I_{off} Ratio
$N_f = 0$	0.42	$8.5x10^3$
$N_f = 1x10^{12}$	0.21	$1.9x10^3$
$N_f = 2x10^{12}$	0.05	$7.3x10^2$
$N_f = -1x10^{12}$	0.63	$1.3x10^4$
$N_f = -2x10^{12}$	0.83	$6x10^4$

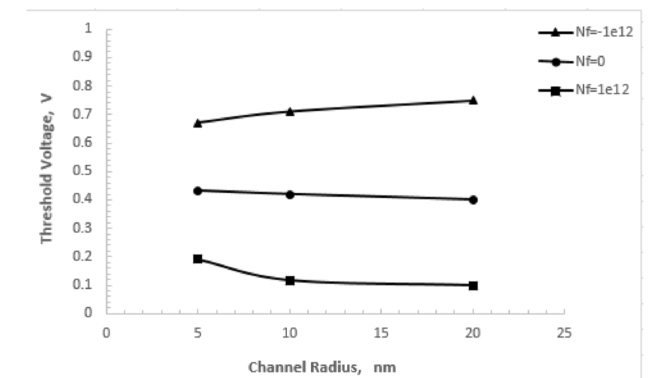

Fig. Threshold Voltage Roll off due to Localised Charges as a Channel Radius.

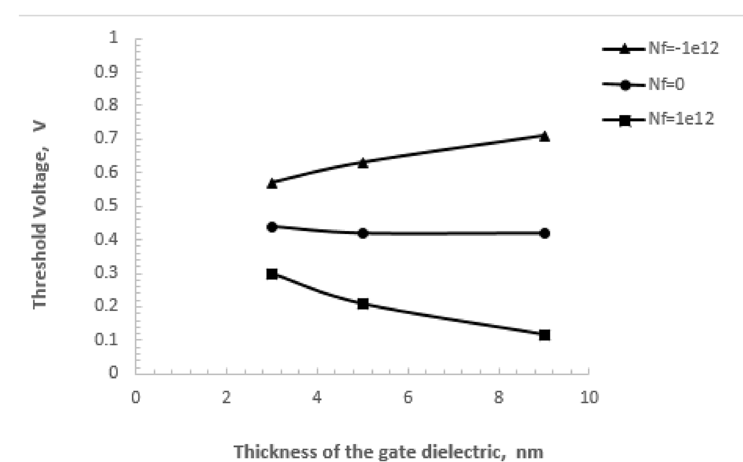

Fig. Threshold Voltage Roll of due to Localised Charges as a function gate dielectric thickness.

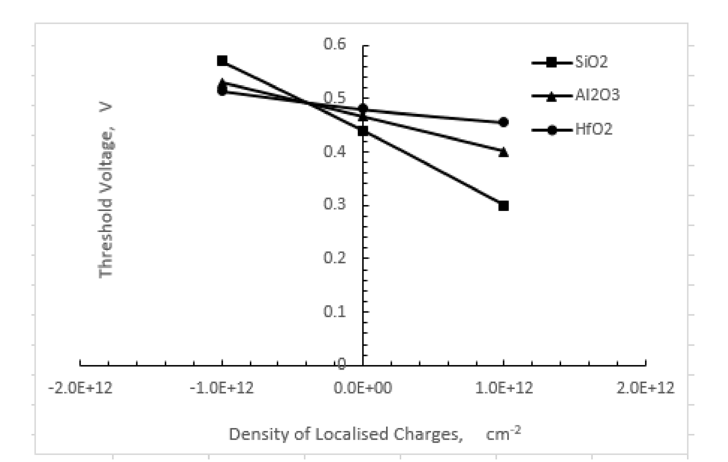

Fig. Effect of High-k Gate Dielectric on the Threshold Voltage Degradation due to Localised charges. Thickness of gate dielectric t_{ox}=5nm.

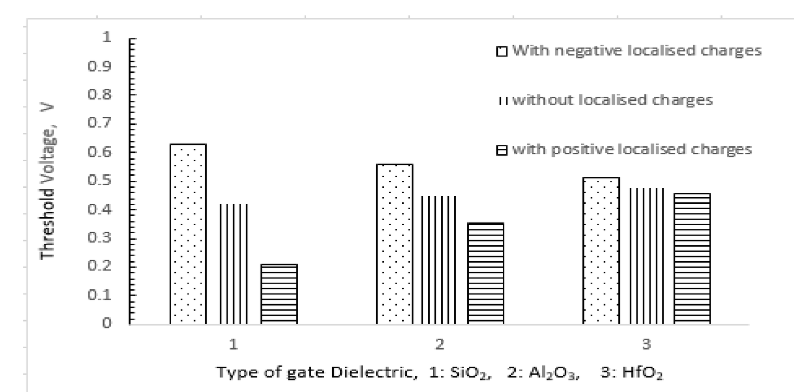

Fig. Threshold Voltage Change due to Localised Charges for different gate dielectrics. Thickness of gate dielectric t_{ox}=9nm.

Conclusions

Major Conclusion drawn from this research work is that device degradation due to localized charges can be reduced using high-k gate dielectrics and thinner gate dielectrics. Using high-k dielectric results in 2.25 times and 8 times less degradation in threshold voltage for Al_2O_3 and HfO_2 gate dielectric respectively as compared to SiO_2. Also device degradation is lesser for thinner gate dielectrics and channel radius has no significant impact on the device degradation. Thus for better reliability against localized charges, thinner gate dielectrics having high k values are more suitable choice in nanoscale devices i.e. Nanowire MOSFET.

References

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3rd International Conference on Recent Trends in Materials Science & Devices (ICRTMD 2025) 24-26 March 2025

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